EUROSOI – ULIS 2020 – 2nd CALL FOR PAPERS

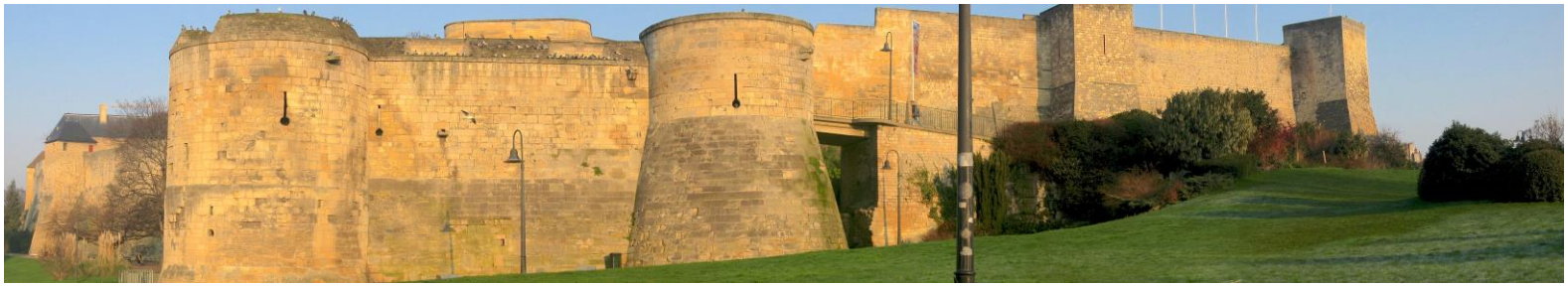
March 31 – April 2, 2020 – Caen, Normandy, France

Social events included in the registration:

- welcome Reception at the Town Hall of Caen
- visit of the old city-center of Caen
- visit of the Mont Saint Michel and its abbey, one of the first UNESCO's " World Heritage sites ".
- visit of the Bayeux Tapestry Museum, a UNESCO's "Memory of the World".

The sixth joint EUROSOI-ULIS conference will be hosted by Normandy University (ENSICAEN, UNICAEN, ESIGELEC) in Caen, inside the William the Conqueror Castel, in the auditorium of Museum of Fine Arts.

The organizing committee invites scientists and engineers working on SOI technology and advanced nanoscale devices to actively participate by submitting high quality, original contributions (2-page abstracts).



The authors of the accepted contributions will be requested to provide a 4-page extended abstract which will be included in the conference proceedings (with IEEE technical sponsorship and ISBN index) and in the IEEE Xplore® digital library. Outstanding papers will be invited for publication in a special issue of Solid-State Electronics. A best paper award will be attributed by the SINANO institute and a best poster award by ELSEVIER. Air France/KLM offers airfare discounts.

Papers in the following areas are solicited:

- **Advanced SOI materials and structures: physical mechanisms and innovative SOI-like devices.**
- **New channel materials for CMOS: strained Si, strained SOI, SiGe, GeOI, III-V and high mobility materials on insulator, carbon nanotubes, graphene and other two-dimensional materials.**
- **Properties of ultra-thin films and buried oxides: defects, interface quality, thin gate dielectrics, high-κ materials for switches and memory.**
- **Nanometer scale devices: technology, characterization techniques and evaluation metrics for high performance, low power, reliability, high frequency and memory applications.**
- **Alternative transistor architectures: FDSOI, Nanowire, FinFET, MuGFET, vertical MOSFET, FeFET and Tunnel FET, MEMS/NEMS, Beyond-CMOS nanoelectronic devices.**
- **New functionalities in silicon-compatible nanostructures and innovative devices representing the More than Moore domain: nanoelectronic sensors, biosensor devices, energy harvesting devices, RF devices, imagers, etc.**
- **CMOS scaling perspectives: device/circuit level performance evaluation, switches and memory scaling; three-dimensional integration of devices and circuits, heterogeneous integration.**
- **Transport phenomena: compact modeling, device simulation, front- and back-end process simulation.**
- **Advanced test structures and characterization techniques: parameter extraction, reliability and variability assessment techniques for new materials and novel devices.**

Abstract submission deadline
January 13, 2020
https://eurosoiulis2020.sciencesconf.org